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STEPHEN B. ACKERMAN
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
LEWIS, MONICA	
ART UNIT	PAPER NUMBER
2822	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,427	LIN ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *69-76 and 78-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *69-76 and 78-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *03/08* .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the after final amendment filed May 22, 2008.

Response to Amendment

2. The finality of that last office action is withdrawn.

Allowable Subject Matter

3. The indicated allowability of claims 77 and 88 are withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Response to Arguments

4. Applicant's arguments with respect to claims 69-76 and 78-90 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s): a) gold seed layer (See Claim 69); and b) electroplated gold layer (See Claim 69). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 80 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contain the following subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention: a) gold layer is connected to said copper pad through said opening in said passivation layer. Applicant stated that support could be found in the specification and drawings. However, the Examiner did not see the support in the places disclosed by Applicant.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 69-71, 80-82 and 87-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. (U.S. Patent No. 6,963,138) in view of Applicant's Prior Art and Raskin et al. (U.S. Patent No. 6,878,633).

In regards to claim 69, Low et al. ("Low") discloses the following:

a) an active device (For Example: See Figure 1);

b) a first dielectric layer (24) (For Example: See Figure 1);

c) an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal laver over said first metal laver and wherein said interconnecting metallization structure comprises a copper pad (16) having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region (For Example: See Figure 1);

d) a second dielectric layer (24) between said first and second metal layers (For Example: See Figure 1);

e) a passivation layer (20) over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region and exposes said first region (For Example: See Figure 1); and

f) an aluminum cap (14) comprising a first portion directly over said first region and a second portion directly over said passivation layer wherein said aluminum cap is connected to said copper pad through said opening in said passivation layer and wherein said aluminum cap has a width greater than that of said opening in said passivation layer (For Example: See Figure 1).

In regards to claim 69, Low fails to disclose the following:

a) a silicon substrate.

However, Applicant's Prior Art ("APA") discloses the use of a silicon substrate (10) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a silicon substrate

as disclosed in APA because it aids in a support for the various components (For Example: See Figure 1).

Additionally, since Low and APA are both from the same field of endeavor, the purpose disclosed by APA would have been recognized in the pertinent art of Low.

b) an adhesion barrier layer on said aluminum cap and a gold layer on said adhesion/barrier laver and directly over said aluminum cap, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer has a thickness between 2 and 20 micrometers and wherein said wire is joined with said gold layer.

However, Raskin et al. ("Raskin") discloses the use of an adhesion barrier layer on said aluminum cap (14) and a gold layer on said adhesion/barrier laver and directly over aluminum cap wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer and wherein said wirebonded wire is joined with said gold layer (For Example: See Figure 14, Column 5 Lines 31-36). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include an adhesion barrier layer on said aluminum cap and a gold layer on said adhesion/barrier laver and directly over aluminum cap wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer and wherein said wirebonded wire is joined with said gold layer as disclosed in Raskin because it aids in providing a structure with a lower cost (For Example: See Abstract).

Additionally, since Low and Raskin are both from the same field of endeavor, the purpose disclosed by Raskin would have been recognized in the pertinent art of Low.

The applicant has not established the critical nature of a "gold layer has a thickness of between about 2um and 20um." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In

such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

Finally, the following limitations make it a product by process claim: a) "electroplated," "seed" and "wirebonded." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claims 70 and 81, Low fails to disclose the following:

a) passivation layer comprises a topmost nitride layer.

However, Raskin discloses the use of a passivation layer that comprises a topmost nitride layer (For Example: See Column 4 Lines 39-43). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include nitride as disclosed in Raskin because it aids in protecting the various components (For Example: See Column 4 Lines 39-43).

Additionally, since Low and Raskin are both from the same field of endeavor, the purpose disclosed by Raskin would have been recognized in the pertinent art of Low.

In regards to claims 71 and 82, Low discloses the following:

a) passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer (For Example: See Column 4 Lines 25 and 26).

In regards to claims 76 and 87, Low fails to disclose the following:

a) gold layer joined with said wirebonded wire is directly over said active device.

However, Raskin discloses the use of a gold layer joined with said wirebonded wire is directly over said active device (For Example: See Figure 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a gold layer joined with said wirebonded wire is directly over said active device as disclosed in Galloway because it aids in providing low cost and high quality integration (For Example: See Abstract and Column 2 Lines 1-11).

Additionally, since Low and Raskin are both from the same field of endeavor, the purpose disclosed by Raskin would have been recognized in the pertinent art of Low.

In regards to claims 78 and 89, Low fails to disclose the following:

a) adhesion/barrier layer comprises titanium.

However, Raskin discloses the use of titanium (For Example: See Column 4 Lines 44-59). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include titanium as disclosed in Raskin because it aids in providing good adhesion (For Example: See Column 4 Lines 44-59).

Additionally, since Low and Raskin are both from the same field of endeavor, the purpose disclosed by Raskin would have been recognized in the pertinent art of Low.

In regards to claim 80, Low discloses the following:

a) an active device (For Example: See Figure 1);

b) a first dielectric layer (24) (For Example: See Figure 1);

c) an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal laver over said first metal laver and wherein said interconnecting metallization structure comprises a copper pad (16) having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region (For Example: See Figure 1);

d) a second dielectric layer (24) between said first and second metal layers (For Example: See Figure 1); and

e) a passivation layer (20) over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region and exposes said first region (For Example: See Figure 1).

In regards to claim 80, Low fails to disclose the following:

a) a silicon substrate.

However, APA discloses the use of a silicon substrate (10) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a silicon substrate as disclosed in APA because it aids in a support for the various components (For Example: See Figure 1).

Additionally, since Low and APA are both from the same field of endeavor, the purpose disclosed by APA would have been recognized in the pertinent art of Low.

b) a gold layer on said adhesion/barrier laver, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer and wherein said wire is joined with said gold layer.

However, Raskin discloses a gold layer on said adhesion/barrier laver, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer and wherein said wire is joined with said gold layer (For Example: See Figure 14 and Column 5 Lines 9-36). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a gold layer on said adhesion/barrier laver, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer and wherein said wire is joined with said gold layer as disclosed in Raskin because it aids in providing a structure with a lower cost (For Example: See Abstract).

Additionally, since Low and Raskin are both from the same field of endeavor, the purpose disclosed by Raskin would have been recognized in the pertinent art of Low.

Finally, the following limitation makes it a product by process claim: a) "electroplated" and "wirebonded." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 88, Low fails to disclose the following:

a) electroplated gold layer has a thickness between 2 and 20 micrometers.

However, the applicant has not established the critical nature of a "gold layer has a thickness of between about 2um and 20um." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art

range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

Finally, the following limitation makes it a product by process claim: a) "electroplated." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

10. Claims 72 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. (U.S. Patent No. 6,963,138) in view of Applicant's Prior Art, Raskin et al. (U.S. Patent No. 6,878,633) and *Silicon Processing* by Wolf et al.

In regards to claims 72 and 83, Low fails to disclose the following:

a) adhesion/barrier layer comprises tantalum.

However, Wolf et al. ("Wolf") discloses the use of tantalum (For Example: See Page 483). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include tantalum as disclosed in Wolf because it is commonly utilized as barrier layers (For Example: See Page 483).

Additionally, since Low and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Low.

11. Claims 73, 74, 84 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. (U.S. Patent No. 6,963,138) in view of Applicant's Prior Art, Raskin et al. (U.S. Patent No. 6,878,633) and *Microchip Fabrication* by Peter Van Zant.

In regards to claims 73 and 84, Low discloses the following:

a) an adhesion/barrier layer and said passivation layer (For Example: See Figure 1).

In regards to claims 73 and 84, Low fails to disclose the following:

a) a polymer layer.

However, Van Zant discloses the use of a polymer layer (For Example: See Page 302). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a polymer layer as disclosed in Van Zant because it is utilized as an interdielectric between metal layers (For Example: See Page 302).

Additionally, since Low and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Low.

Finally, the applicant has not established the critical nature of a "polymer layer has a thickness of between about 2um and 20um." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

In regards to claims 74 and 85, Low discloses the following:

a) an adhesion/barrier layer and said passivation layer (For Example: See Figure 1).

In regards to claims 74 and 85, Low fails to disclose the following:

a) a polyimide layer.

However, Van Zant discloses the use of polyimide (For Example: See Page 302). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a polyimide as disclosed in Van Zant because it is utilized as an interdielectric between metal layers (For Example: See Page 302).

Additionally, since Low and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Low.

12. Claims 75 and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. (U.S. Patent No. 6,963,138) in view of Applicant's Prior Art, Raskin et al. (U.S. Patent No. 6,878,633) and Hashimoto (U.S. Patent No. 6,383,916).

In regards to claims 75 and 86, Low fails to disclose the following:

a) a third dielectric layer on said layer, wherein an opening in said dielectric layer is over said gold layer joined with said wirebonded wire.

However, Hashimoto discloses the use of a third dielectric layer (165) on said layer, wherein an opening in said dielectric layer is over said gold layer joined with said wirebonded wire (For Example: See Figure 14C). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a third dielectric layer on said layer, wherein an opening in said dielectric layer is over said gold layer joined with said wirebonded wire as disclosed in Hashimoto because it aids in protecting the components (For Example: See Figure 14C).

Additionally, since Low and Hashimoto are both from the same field of endeavor, the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Low.

13. Claims 79 and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. (U.S. Patent No. 6,963,138) in view of Applicant's Prior Art, Raskin et al. (U.S. Patent No. 6,878,633) and Lin (U.S. Patent No. 6,383,916).

In regards to claims 79 and 90, Low fails to disclose the following:

a) the device comprises a transistor.

However, Lin discloses the use of a transistor (For Example: See Column 3 Lines 45-47). It would have been obvious to one having ordinary skill in the art at the time the invention was

made to modify the semiconductor of Low to include a transistor as disclosed in Lin because it aids in the formation of an integrated circuit (For Example: See Abstract).

Additionally, since Low and Lin are both from the same field of endeavor, the purpose disclosed by Lin would have been recognized in the pertinent art of Low.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization

where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

/Monica Lewis/
Primary Examiner, Art Unit 2822

June 11, 2008